



SPD15P10PL G

SIPMOS® Power-Transistor

Features

- P-Channel
- Enhancement mode
- logic level
- Avalanche rated
- Pb-free lead plating; RoHS compliant
- Qualified according to AEC Q101

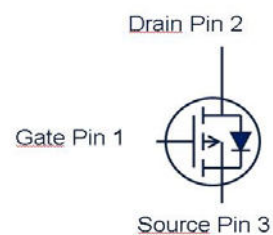
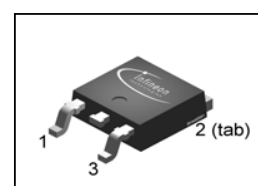


Type	Package	Marking	Lead free	Packing
SPD15P10PL G	PG-TO252-3	15P10PL	Yes	Non dry

Product Summary

V_{DS}	-100	V
$R_{DS(on),max}$	0.20	Ω
I_D	-15	A

PG-TO252-3



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	-15	A
		$T_C=100\text{ °C}$	11.3	
Pulsed drain current	$I_{D,pulse}$	$T_C=25\text{ °C}$	-60	
Avalanche energy, single pulse	E_{AS}	$I_D=-15\text{ A}$, $R_{GS}=25\text{ }\Omega$	230	mJ
Gate source voltage	V_{GS}		± 20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	128	W
Operating and storage temperature	T_j , T_{stg}		-55 ... 175	°C
ESD Class			1C (1kV to 2kV)	
Soldering temperature			260 °C	
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - soldering point	R_{thJC}		-	-	1.17	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint, steady state	-	-	75	
		6 cm ² cooling area ¹⁾ , steady state	-	-	45	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=-250\text{ mA}$	-100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=-1.54\text{ mA}$	-1	-1.5	-2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-0.1	-1	μA
		$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	-10	-100	
Gate-source leakage current	I_{GSS}	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$	-	-10	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}$, $I_D=-9.7\text{ A}$	-	190	270	$\text{m}\Omega$
		$V_{GS}=-10\text{ V}$, $I_D=-11.3\text{ A}$	-	140	200	$\text{m}\Omega$
Transconductance	g_{fs}	$ V_{DS} > 2 I_D R_{DS(on)max}$, $I_D=-11.3\text{ A}$	5.5	11.0	-	S

¹⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.


SPD15P10PL G

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	1120	1490	pF
Output capacitance	C_{oss}		-	272	362	
Reverse transfer capacitance	C_{rss}		-	120	180	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-50\text{ V}, V_{GS}=-10\text{ V}, I_D=-15\text{ A},$ $R_G=6\ \Omega$	-	7.6	11	ns
Rise time	t_r		-	21	31	
Turn-off delay time	$t_{d(off)}$		-	50	75	
Fall time	t_f		-	29	44	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-80\text{ V}, I_D=-15\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	4.3	5.7	nC
Gate to drain charge	Q_{gd}		-	17	26	
Gate charge total	Q_g		-	47	62	
Gate plateau voltage	$V_{plateau}$		-	4.0	-	V

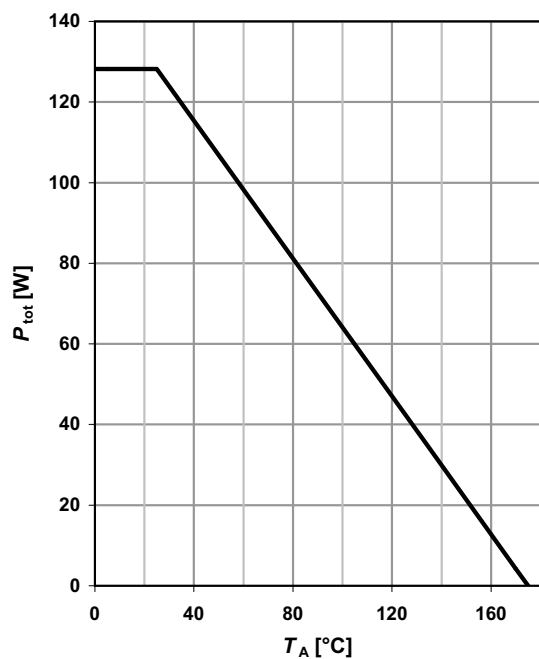
Reverse Diode

Diode continuous forward current	I_S	$T_C=25\text{ °C}$	-	-	-15	A
Diode pulse current	$I_{S,pulse}$		-	-	-60	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-15\text{ A},$ $T_j=25\text{ °C}$	-	-0.96	-1.35	V
Reverse recovery time	t_{rr}	$V_R=50\text{ V}, I_F= I_S ,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	110	165	ns
Reverse recovery charge	Q_{rr}		-	450	675	nC

²⁾ See figure 16 for gate charge parameter definition

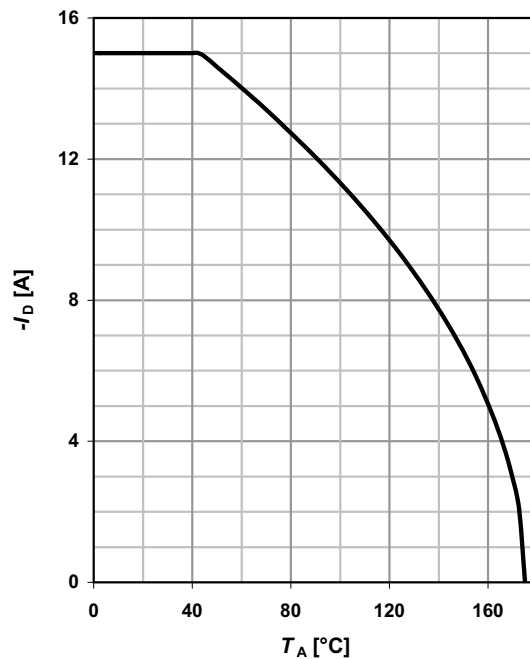
1 Power dissipation

$$P_{\text{tot}} = f(T_C)$$



2 Drain current

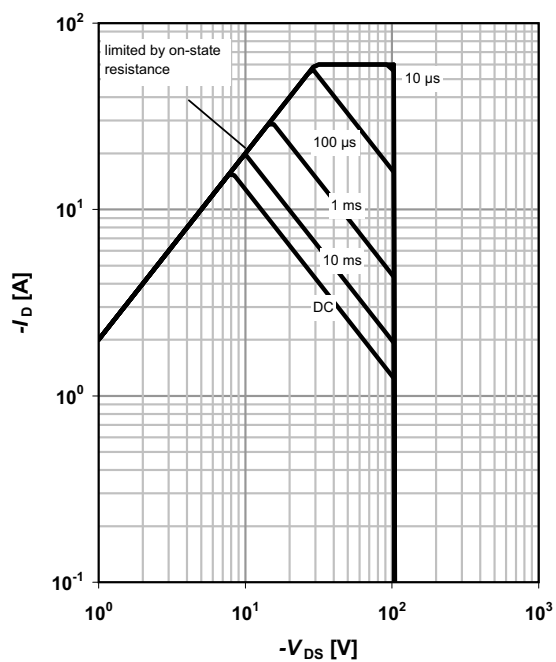
$$I_D = f(T_C); |V_{GS}| \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

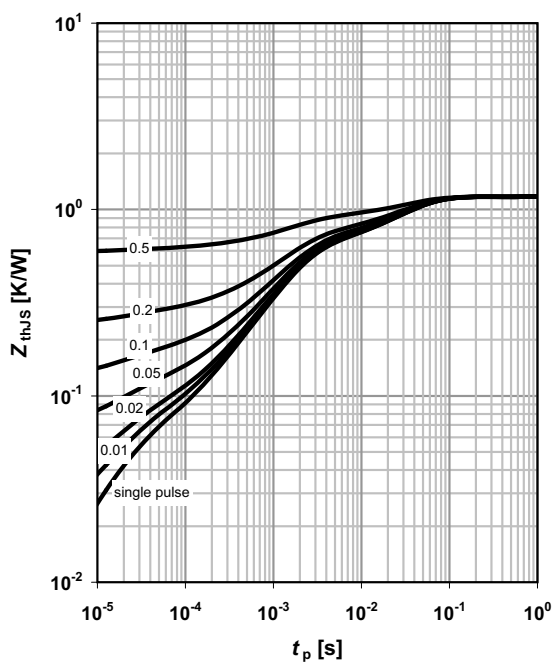
parameter: t_p



4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



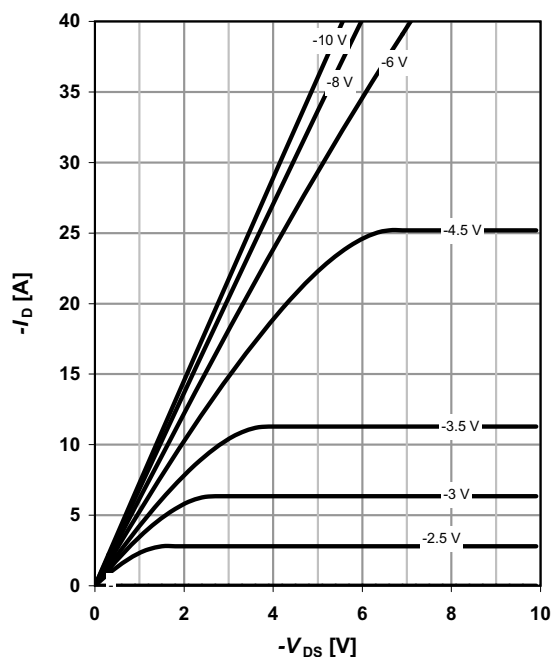


SPD15P10PL G

5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

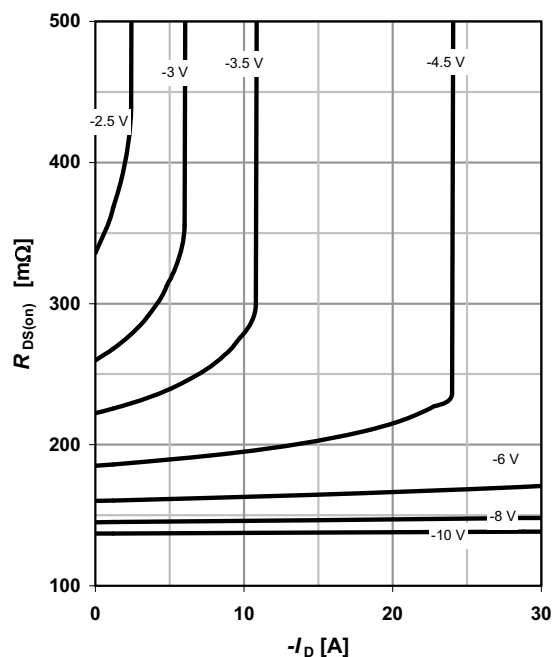
parameter: V_{GS}



6 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$$

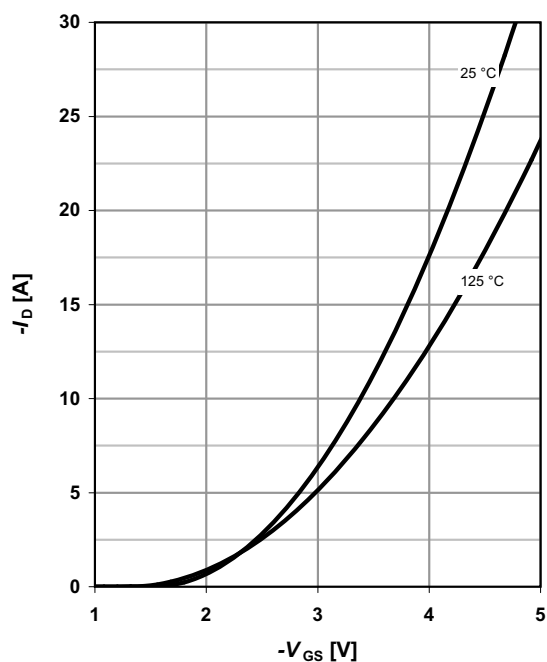
parameter: V_{GS}



7 Typ. transfer characteristics

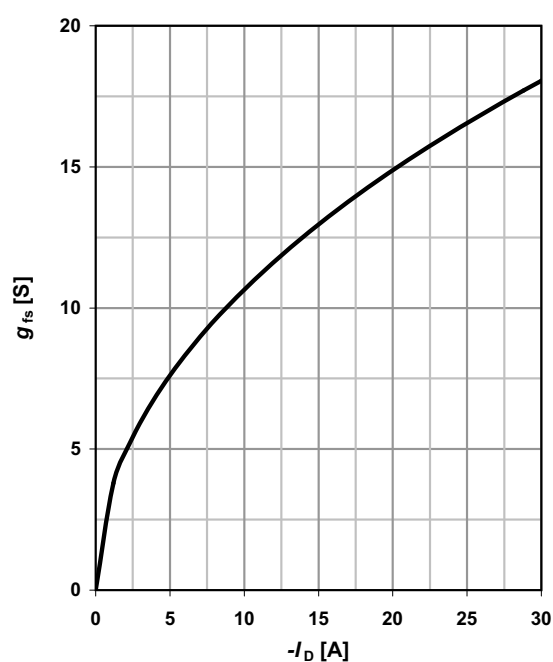
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$$

parameter: T_j



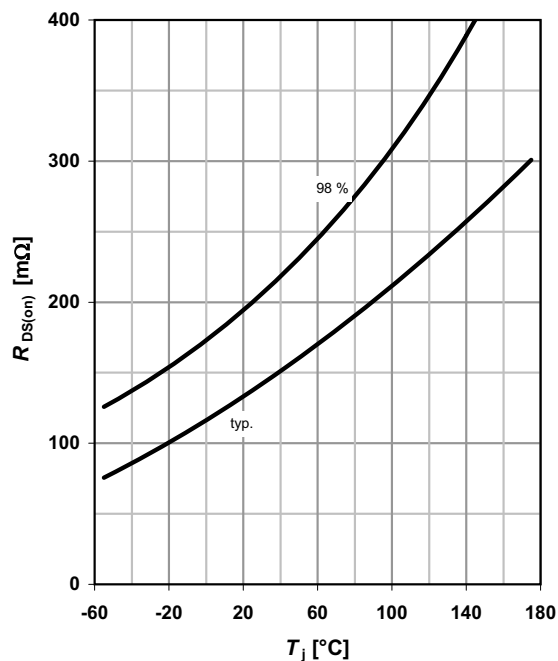
8 Typ. forward transconductance

$$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$$



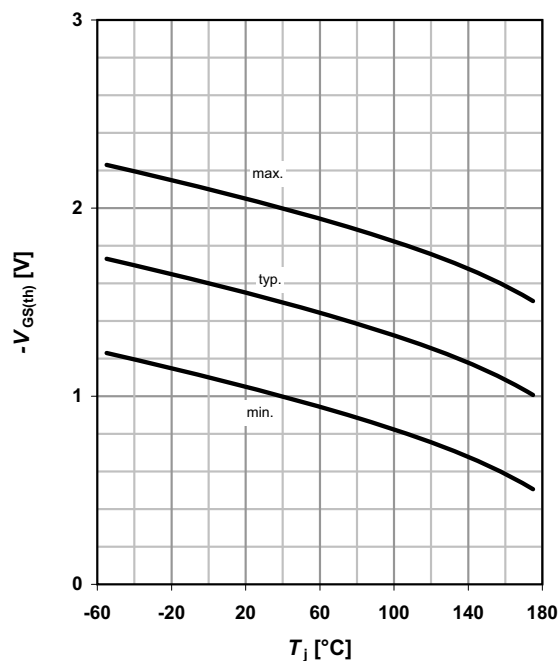
9 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j); I_D = -11.3 \text{ A}; V_{GS} = -10 \text{ V}$$



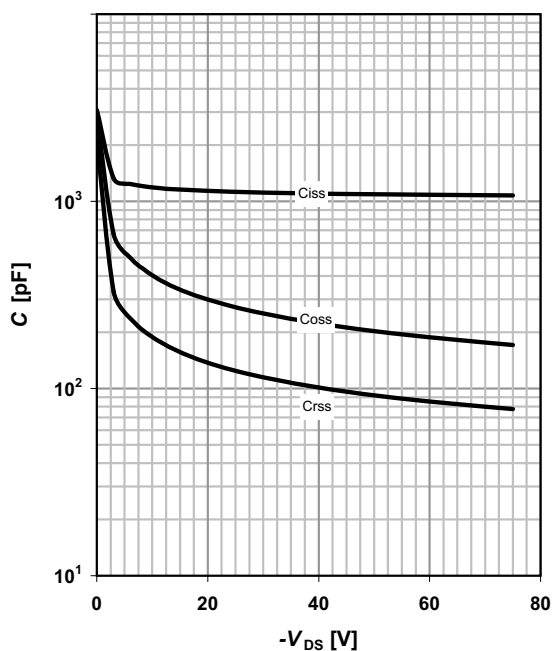
10 Typ. gate threshold voltage

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = -1.54 \text{ mA}$$



11 Typ. capacitances

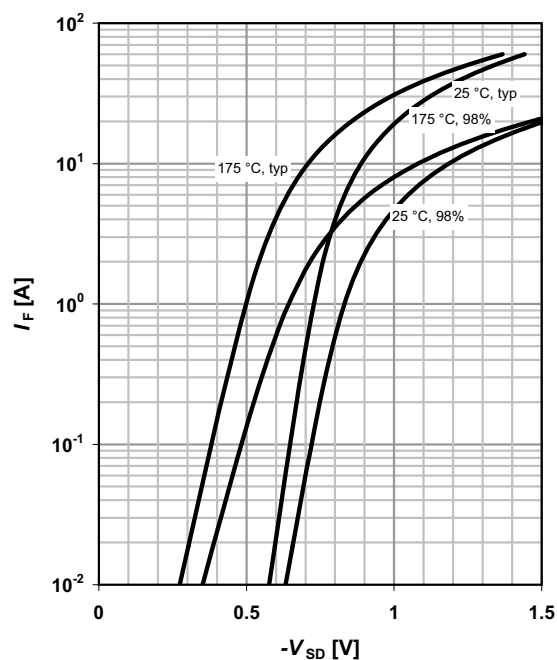
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

parameter: T_j



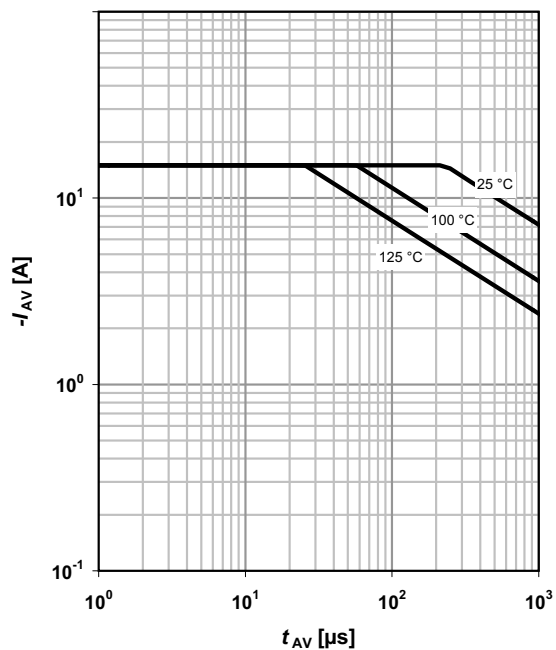


SPD15P10PL G

13 Avalanche characteristics

$$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$$

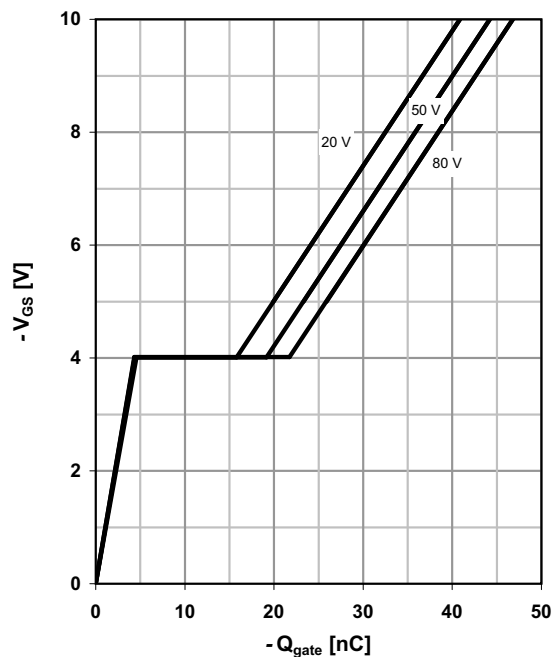
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

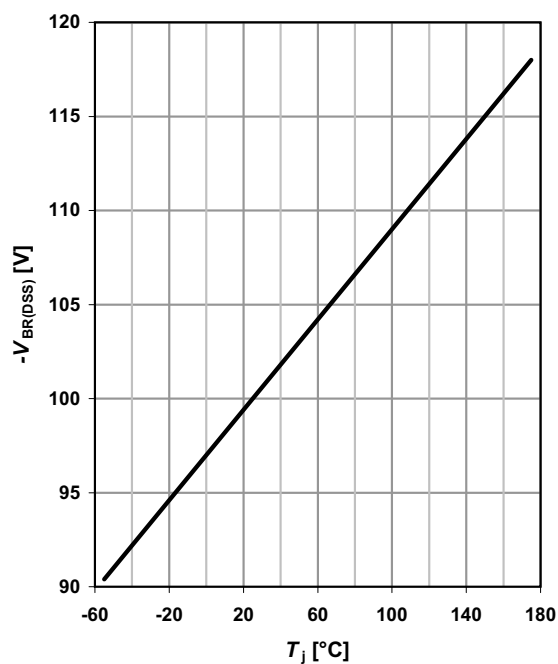
$$V_{GS}=f(Q_{\text{gate}}); I_D=-15\ \text{A pulsed}$$

parameter: V_{DD}

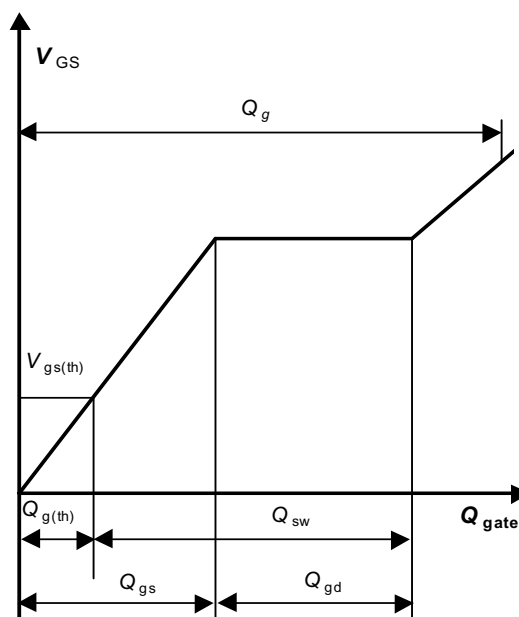


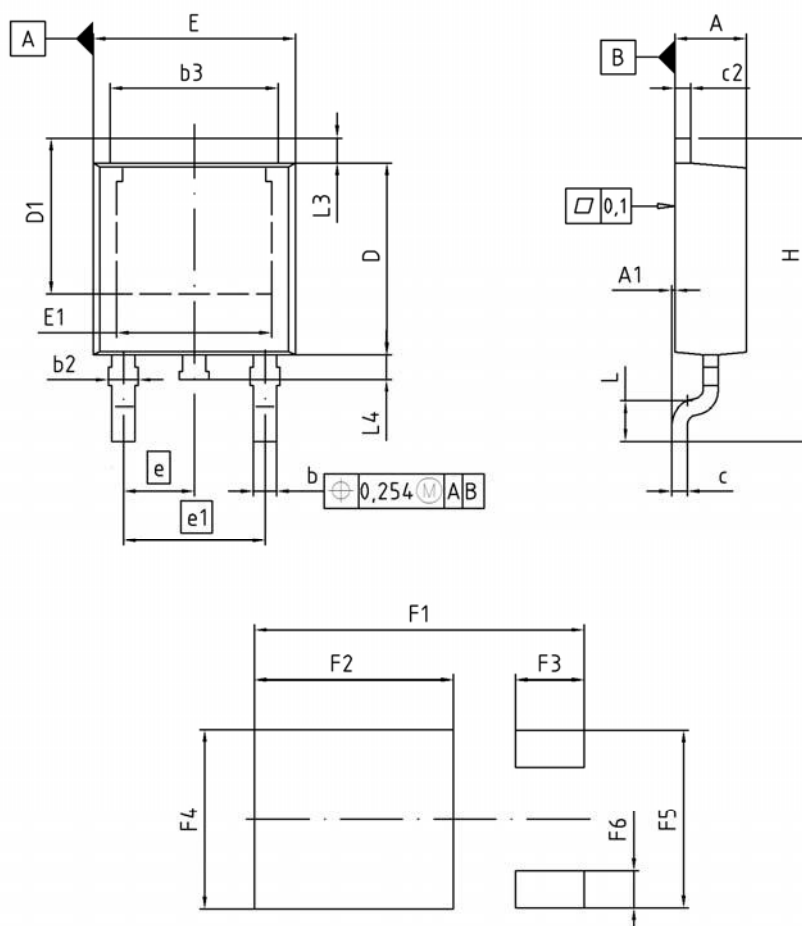
15 Drain-source breakdown voltage

$$V_{BR(DSS)}=f(T_j); I_D=-1\ \text{mA}$$

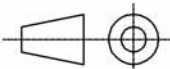


16 Gate charge waveforms



Package Outline: PG-TO-252-3


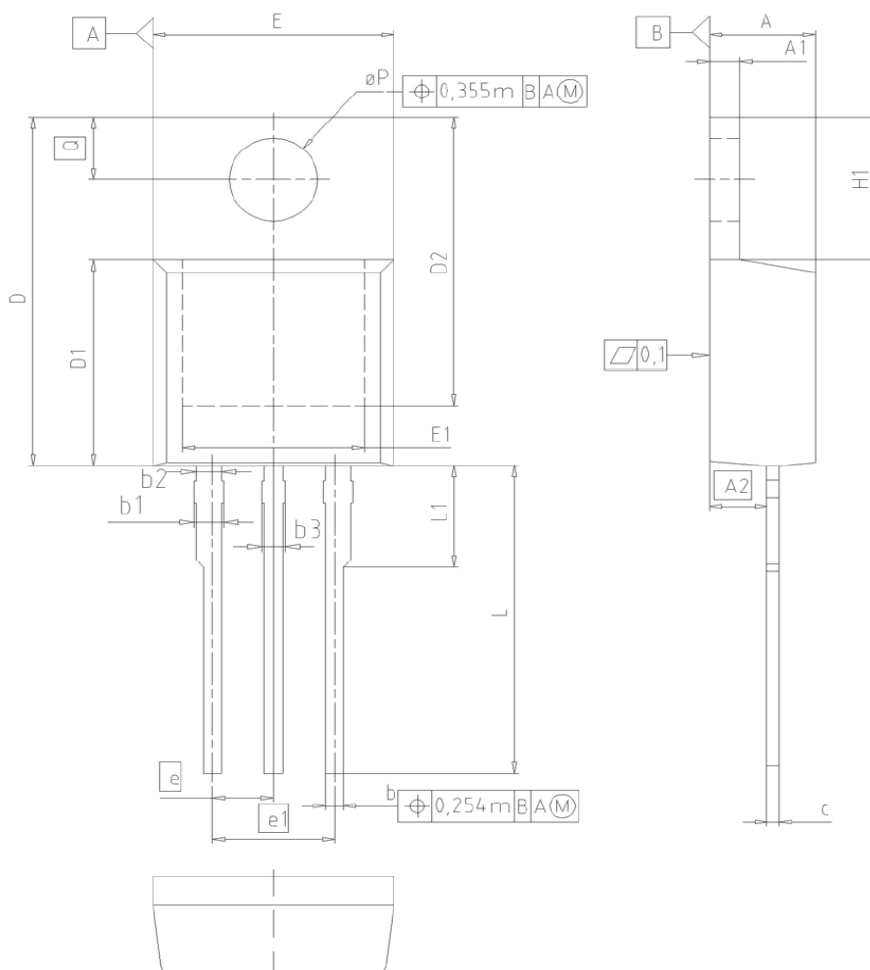
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29		0.090	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.50	10.70	0.413	0.421
F2	6.30	6.50	0.248	0.256
F3	2.10	2.30	0.083	0.091
F4	5.70	5.90	0.224	0.232
F5	5.66	5.86	0.223	0.231
F6	1.10	1.30	0.043	0.051

DOCUMENT NO. Z8B00003328
SCALE 0 2.0 4mm
EUROPEAN PROJECTION 
ISSUE DATE 19-10-2007
REVISION 03



SPD15P10PL G

PG-TO220-3: Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
øP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO. Z8B00003318
SCALE 0 2.5 5mm
EUROPEAN PROJECTION
ISSUE DATE 23-08-2007
REVISION 05

Published by
Infineon Technologies AG
81726 Munich, Germany
© 2008 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.